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EXAMINER	
WANG, JUE S	

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/599,593	DUTT ET AL.	
	Examiner	Art Unit	
	JUE WANG	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-27 have been examined.

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 12-23 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

4. Claims 12-23 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. In claims 12-23, a "generic instruction model" is recited; however, it appears that the generic instruction model would reasonably be interpreted by one of ordinary skill in the art as software, per se, since the instruction specification and operation classes recited as part of the generic instruction model would reasonably be interpreted by one of ordinary skill in the art as software, per se. While claim 12 does recite that the generic instruction model is stored on a computer readable medium and read by a processor, the computer readable medium and the processor is not recited as part of the generic instruction model. Therefore, the generic instruction model of claims 12-23 is still reasonably interpreted as functional descriptive material, per se, failing to be tangibly embodied or include any recited hardware as part of the generic instruction model and thereby fit that statutory category of invention.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 9, 10, 24, 26, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leupers et al. "Generation of Interpretive and Compiled Instruction Set Simulators" (hereinafter Leupers), in view of Zemach et al. (US 7,107,580, hereinafter Zemach).

7. As per claim 1, Leupers teaches the invention as claimed, including a method of simulating an instruction set architecture (ISA) with a instruction set simulator (ISS), comprising:

fetching a first decoded instruction during a run time, wherein the decoded instruction is decoded from an original instruction in a target application program during a compile time preceding the run time (i.e., each instruction of a machine program is decoded at compile time, see page 340, Fig 1, page 342, section 4.3), the decoded instruction pointing to a template configured to implement the functionality of the instruction (i.e., generating C macro calls to generic simulation functions, see page 341, section 4.1, 4.2), ; and

executing the designated template (see page 342, section 4.5).

Leupers does not teach determining whether the fetched instruction is modified from the original instruction and executing the designated template if the instruction was not modified.

Zemach teaches a method of binary translation that determines whether fetched instruction is modified from an original instruction and executes the translation of the fetched instruction if the instruction as not modified (see Fig 3, column 2, lines 51-64).

It would have been obvious to one of ordinary skill in the art at the time of the to have modified Leupers to determine whether the fetched instruction is modified from the original instruction and executing the designated template if the instruction was not modified as similarly taught by Zemach to detect self-modifying code which renders a previous translation of an instruction obsolete after the instruction is modified (see column 1, lines 64 - column 2, line 5, column 2, line 65 – column 3, line 10 of Zemach).

8. As per claim 9, Leupers does not teaches re-decoding the fetched instruction during the run time if the fetched instruction was modified, wherein the re-decoded instruction designates a function configured to implement the functionality of the instruction; and executing the designated function if the instruction was modified.

Zemach teaches re-decoding the fetched instruction during the run time if the fetched instruction was modified, wherein the re-decoded instruction designates a function configured to implement the functionality of the instruction; and executing the designated function if the instruction was modified (see Fig 3, Fig 4, column 1, lines 56-63, column 2, line 51-column 3, line 10).

It would have been obvious to one of ordinary skill in the art at the time of the to have modified Leupers to re-decode the fetched instruction during the run time if the fetched instruction was modified, wherein the re-decoded instruction designates a function configured to implement the functionality of the instruction; and execute the designated function if the instruction was modified as similarly taught by Zemach because self-modifying code must be re-translated since the modification renders a previous translation of an instruction obsolete (see column 1, lines 64 - column 2, line 5, column 2, line 65 – column 3, line 10 of Zemach).

9. As per claim 10, Zemach teaches executing the modified instructions using an interpretive process (see column 2, line 65 – column 3, line 10).

10. As per claims 24, 26, and 27, these are the computer readable medium claims of claims 1, 9, and 10. Therefore, they are rejected using the same reasons as claims 1, 9, and 10.

11. Claims 2 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leupers et al. "Generation of Interpretive and Compiled Instruction Set Simulators" (hereinafter Leupers), in view of Zemach et al. (US 7,107,580, hereinafter Zemach), further in view of Simpson (US 4,794,522).

12. As per claim 2, Leupers teaches decoding the original instruction by selecting a template corresponding to the original instruction and customizing the template prior to fetching the instruction (see page 341, sections 4.1, 4.2).

Leupers does not explicitly teach that the customization is based on the data in original instruction.

Simpson teaches customization of templates based on the data in original instruction (see column 2, lines 11-14).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have modified Leupers such that the customization is based on data in the original instruction as taught by Simpson to improve runtime by building in references to the proper registers, addresses, etc. present in the specific instance of the target instruction (see column 2, lines 11-30 of Simpson).

13. As per claim 5, Simpson teaches wherein the customizing the template comprises determining a value of a parameter in the template based on the data in the original instruction (see column 2, lines 11-14).

14. Claims 3, 4, 6-8, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leupers et al. "Generation of Interpretive and Compiled Instruction Set Simulators" (hereinafter Leupers), in view of Zemach et al. (US 7,107,580, hereinafter Zemach), further in view of Simpson (US 4,794,522), further in view of DeWitt, Jr. et al. (US 2005/0102493 A1, hereinafter DeWitt).

15. As per claim 3, Leupers teaches wherein the template corresponds to a first class of one or more instructions (see page 341, sections 4.1, 4.2), wherein the template has a corresponding value usable to identify instructions belonging to that class (i.e., case labels, see page 342, section 4.5).

Leupers does not teach the use of a corresponding mask usable to identify instructions belonging to that class.

DeWitt is cited to teach the use of a mask usable to identify instructions belonging to an operation class (see at least [0189]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have modified Leupers to use an operation mask usable to identify instructions belonging to an operation class as taught by DeWitt because the method chose to identify a type of instruction is a design choice and the use of an operation mask is a well known way of identifying a type of instructions (see [0189] of DeWitt).

16. As per claim 4, Leupers teaches comparing the original instruction to the value corresponding to the template; and selecting the template if the value matches the original instruction (see page 342, section 4.5).

Leupers does not teach wherein the use of a mask.

DeWitt is cited to teach the use of a mask usable to identify instructions belonging to an operation class (see at least [0189]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have modified Leupers to use a mask usable to identify instructions belonging to an operation class as taught by DeWitt because the method chose to identify

a type of instruction is a design choice and the use of an operation mask is a well known way of identifying a type of instructions (see [0189] of DeWitt).

17. As per claim 6, Simpson teaches wherein the customizing the template comprises determining a value of a parameter in the template based on the data in the original instruction (see column 2, lines 11-14).

18. As per claim 7, Leupers as modified teaches compiling a first program comprising the customized template in the compile time (see page 340, Figure 1, page 341, section 4.3).

19. As per claim 8, Leupers teaches optimizing the template during compile time (i.e., the simulation functions can be replaced by faster macros, see page 341, section 4.1).

20. As per claim 11, Leupers teaches compiling the target application program to generate the original instructions (see page 341, section 4.3).

21. Claims 12-16, 18, 19, 22, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Killian et al. (US 6,477,683 B1, hereinafter Killian), in view of DeWitt, Jr. et al. (US 2005/0102493 A1, hereinafter DeWitt).

22. As per claim 12, Killian teaches the invention as claimed, including a generic instruction model stored on a computer readable medium, which when read by a

processor is for use in a instruction set architecture (ISA) simulator (i.e., configuring a simulator for a specific instruction set architecture using a ISA definition, see Fig 6, column 6, line 65 – column 7, line 20, column 17, line 48 – column 18, line 1, column 31, lines 50-61), comprising:

an instruction specification usable to interpret each instruction in an ISA, the instruction specification comprising one or more operation classes (i.e., the instruction class statement iclass, see column 14, line 10 - column 16, line 45);

wherein each operation class defining a set of one or more instructions (i.e., instruction semantic statement describes the behavior of one or more instructions, see column 16, lines 14-45), the operation class having a list usable to identify instructions belonging to the class (see column 16, lines 45-50); and

further wherein the operation class comprises one or more symbols and an expression describing the class in terms of the one or more symbols (i.e., instruction semantic statement defines the opcode and operands of the instructions, the see column 16, lines 14-67), each symbol having a corresponding set of one or more symbol types, each symbol type in the set comprising information usable to determine the symbol when compared to an instruction (i.e., instruction operand statements identify registers and immediate constants, see at least column 14, lines 30-62, column 15, lines 14-36, column 16, lines 53-67).

Killian does not explicitly teach using an operation mask usable to identify instructions belonging to an operation class.

DeWitt is cited to teach the use of an operation mask usable to identify instructions belonging to an operation class (see at least [0189]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have modified Killian to use an operation mask to identify instructions belonging to an operation class because it is well known in the art that the use of an operation mask is another alternative to using a list to identify a type of instructions (see [0189] of DeWitt) and the use of a mask is well known to have the advantage of having a smaller storage requirement than a list.

23. As per claim 13, Killian teaches wherein the set of instructions has a common behavior and the expression defines the behavior of the class in terms of the one or more symbols (i.e., instruction semantic statement describes the behavior of one or more instructions, see column 16, lines 14-45).

24. As per claim 14, Killian teaches wherein one symbol type in the type set is a constant type (i.e., instruction operand statements operand identify registers and immediate constants, see at least column 15, lines 14-36).

25. As per claim 15, Killian teaches wherein the type set comprises a plurality of constant types, each constant type having a corresponding type mask usable to determine the constant when compared to an instruction (see column 14, lines 30-62, column 15, line 14 - column 16, line 13).

26. As per claim 16, Killian teaches wherein one symbol type in the type set is a register type (i.e., instruction operand statements operand identify registers and immediate constants, see at least column 15, lines 14-36).

27. As per claim 18, Killian teaches wherein one symbol type in the type set is an operation type (see column 14, lines 30-62, column 16, lines 53-67).

28. As per claim 19, Killian teaches wherein the type set comprises a plurality of operation types, each operation type having a corresponding type mask usable to determine the operation when compared to an instruction (i.e., the bits 20-23 in an instruction define the opcode, see column 14, lines 30-62, column 15, lines 1-5, column 16, lines 60-53-67).

29. As per claim 22, Killian teaches wherein each instruction comprise a series of binary data values (see at least column 14, lines 30-67).

DeWitt teaches the operation mask comprises a series of mask positions wherein each mask position corresponds to one instance of a binary data value (see at least [0189]).

30. As per claim 23, DeWitt teaches wherein each mask position has a value selected from a group comprising: a binary one value, a binary zero value and a do not care value (see [0189]).

31. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Killian et al. (US 6,477,683 B1, hereinafter Killian), in view of DeWitt, Jr. et al. (US 2005/0102493 A1, hereinafter DeWitt), further in view of Nohl et al. (US 2003/0217248 A1, hereinafter Nohl).

32. As per claim 17, Killian does not explicitly teach wherein the register type comprises a register index and a register class.

Nohl teaches a processor description for an instruction that includes a register type comprising a register index and a register class (see Fig 5, [0050], [0051]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have modified Killian to include a register type comprising a register index and a register as taught by Nohl because the specification description for an instruction is a design choice.

33. Claims 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Killian et al. (US 6,477,683 B1, hereinafter Killian), in view of DeWitt, Jr. et al. (US 2005/0102493 A1, hereinafter DeWitt), further in view of Wang et al. (US 2005/0160402 A1, hereinafter Wang).

34. As per claim 20, Killian teaches wherein the at least one operation class comprises a plurality of expressions (see column 16, line 40 - column 17, line 26).

Killian and DeWitt do not explicitly teach wherein each expression being conditional on data within an instruction.

Wang teaches an operation class comprises a plurality of expressions where each expression conditional on data within an instruction (see [0110]-[0112]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have modified Killian and DeWitt to provide an operation class where each expression being conditional on data within an instruction as taught by Wang because the invention of Killian is usable to extend and customize the processor instruction set (see column 6, lines 43-64 of Killian) and it is advantageous to extend a processor instruction set with the conditional instruction as taught by Wang to reduce the number of operations that are performed (see [0110]-[0112] of Wang).

35. As per claim 21, Killian and DeWitt do not explicitly teach wherein each instruction comprises a series of slots, each slot comprising data translatable into an operation.

Wang teaches an instruction specification wherein each instruction comprises a series of slots, each slot comprising data translatable into an operation (see [0035], [0036], [0055]-[0080]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have modified Killian and DeWitt to provide an instruction comprises a series of slots, each slot comprising data translatable into an operation as taught by Wang because the invention of Killian is usable to extend and customize the processor instruction set (see column 6, lines 43-64 of Killian) and it is advantageous to extend a processor instruction set to include instruction with a series of slots to allow parallel execution of operations (see [0007], [0035] of Wang).

36. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Leupers et al. "Generation of Interpretive and Compiled Instruction Set Simulators" (hereinafter Leupers), in view of Zemach et al. (US 7,107,580, hereinafter Zemach), further in view of DeWitt, Jr. et al. (US 2005/0102493 A1, hereinafter DeWitt).

37. As per claim 25, Leupers teaches wherein the template corresponds to a first class of one or more instructions (see page 341, sections 4.1, 4.2), wherein the template has a corresponding value usable to identify instructions belonging to that class (i.e., case labels, see page 342, section 4.5).

Leupers does not teach wherein the use of a corresponding mask usable to identify instructions belonging to that class.

DeWitt is cited to teach the use of a mask usable to identify instructions belonging to an operation class (see at least [0189]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have modified Leupers to use an operation mask usable to identify instructions belonging to an operation class as taught by DeWitt because the method chose to identify a type of instruction is a design choice and the use of an operation mask is a well known way of identifying a type of instructions (see [0189] of DeWitt).

Response to Arguments

38. Rejection of claims under §101:

39. As per the rejection of claims 12-23, Examiner notes that the current claim amendments do not overcome the 101 rejection. While claim 12 has been amended to

recite that the generic instruction model is stored on a computer readable medium and read by a processor, the computer readable medium and the processor is not recited as part of the generic instruction model. Therefore, the recited generic instruction model of claims 12-23 is still reasonably interpreted as functional descriptive material, per se, because the generic instruction model does not include any hardware.

40. Rejection of claims under §102(b):

41. Examiner has withdrawn the prior §102(b) rejection using prior art Reshadi et al., "A Framework for Fast, Flexible and Retargetable Instruction-Set Architecture Simulation" in light of Inventors' affidavits.

Conclusion

42. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Jennings et al. (US 7,058,932 B1) is cited to teach a method for emulation of computer programs.
- Diep et al. "WMW: A Visualization-Based Microarchitecture Workbench", 1995, Computer, volume 28, issue 2.
- V. Rajesh, "A Generic Approach to Performance Modeling and Its Application to Simulator Generator", August 1998, Masters Thesis, Department of Computer Science & Engineering, Indian Institute of Technology Kanpur.

- Amicel et al. "Matering Startup costs in Assembler-Based Compiled Instruction-Set Simulation", 2002, Proceedings of the Sixth Annual Workshop on Interaction between Compilers and Computer Architectures.

43. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jue S. Wang whose telephone number is (571) 270-1655. The examiner can normally be reached on M-F 9:30 am - 5:00pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lewis Bullock can be reached on 571-272-3759. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lewis A. Bullock, Jr./
Supervisory Patent Examiner, Art Unit 2193

Jue Wang
Examiner
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